Acta of Turin Polytechnic University in Tashkent, 2023, 30, 20-24
Published Online September 2023 in Acta TTPU (http://www.acta.polito.uz/)

EFFICIENT IMPLEMENTATION OF A BUCK CONVERTER CONTROL USING A LOW PERFORMANCE MICROCONTROLLER

Francesco Gregoretti* **and Maksudjon Usmonov**
Turin Polytechnic University in Tashkent, Uzbekistan
*Email: francesco.gregoretti@polito.uz

Abstract– The implementation of power switching converters by low-cost embedded systems is in general limited by the low operating frequency as well as the resolution of the variable duty cycle waveform which controls the power converter. The paper analyzes how the use of dedicated hardware units may partially overcome these limits and whether a microcontroller in an embedded system may both operate as a power supply controller and at the same time perform other application tasks which do require a limited amount of processing power.

Key words– component, formatting, style, styling, insert (key words)

I INTRODUCTION

A number of simple applications mapped to embedded systems require both to control a subsystem to control and the same time to generate a voltage source different from the main supply and in battery operated devices the conversion task must be efficient. Often the processing power required for the control task is limited and for a large part of the time the processor is idle even with a simple architecture. If the application where the processor is embedded requires power conversion from/to different sources the control and the power generation tasks may be performed in parallel.

In order to evaluate the feasibility of such an approach we decided to implement a test system and to perform a number of measurements to identify the limits of power regulation by a microcontroller and the processing power required.

The organization of the paper is the following one. Section II describes the experimental testbench used. Section III briefly reviews the main parameters of a switching converter and the description of the design choices taken in the experiment.

Section IV describes the results of the measurements and finally section V will derive some conclusions and suggest possible further investigations

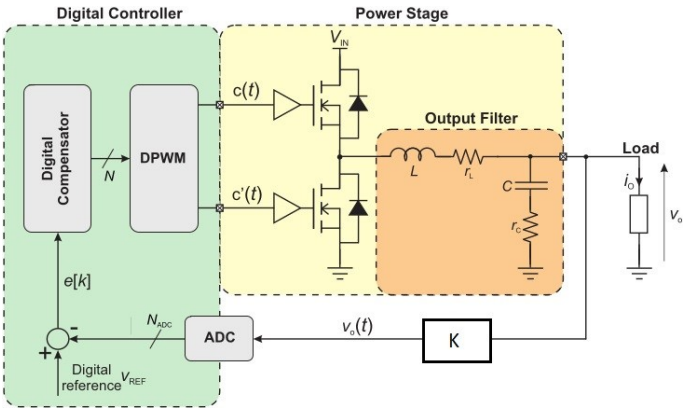

Fig. 1: The experimental testbench.

II THE EXPERIMENTAL TESTBENCH

The structure of the experimental testbench is shown in fig.1. The two main blocks are the Digital Controller and a Power Stage which is controlled by means of a Digital Pulse Width Modulator (DPWM).

A. The Digital controller

In order to demonstrate the feasibility of the approach we decided to start from a well-known but performance limited microcontroller system. In the frame of the development of teaching modules for power electronics, we chose a simple Arduino Uno board [1] which includes a 10bit Analog to Digital Converter (ADC) with a reference voltage VREF equal to 5 V. The core is an ATmega328P processor with a 16 MHz clock, corresponding to an average instruction time of 0.1 us and a number of peripherals among which a timer unit that may be configured as DPWM as better described in the next section.

B. The power stage The power stage is a synchronous buck

power converter developed in a previous project composed of two power switches, driven by the two non-overlapping outputs of the DPWM, an inductor and an output filter capacitor.

The value L is 100 mH and the value of C is 220 mF giving a characteristic resonant frequency of the filter of approximately 1 kHz. The parasitic series resistance rC of the capacitor is 90 mW. The system is designed to operate with an input voltage varying from 10 to 18 V and the digital reference may be set for an output voltage from 2V to 10V and the maximum output current is 2 A. The load resistance used in the experiments has been 100 W.

The output voltage is scaled down by a factor **K** in order to make the input voltage to the ADC always lower than the reference voltage of the ADC itself even in the worst condition when $V_o = V_{in}$ which may happen if the upper switch is always closed.

III DESIGN AND PARAMETERS

The operation of a switching buck converter is quite straightforward. The DPWM sets the duty cycle D of a square wave which opens and closes the power switches in such a way that a fraction of the input voltage V_{in} is filtered by the LC output filter and becomes the output voltage V_o. If the frequency of the square wave is far higher than the cutoff frequency of the filter, then V_o is almost constant and equal to:

$$V_o = D \cdot V_{in} \tag{1}$$

The period of the square wave with variable duty cycle is referred to as *switching cycle.*

The compensator in the digital controller has the task to compare the input value of the ADC to a digital reference setting the value of the output voltage and to set the value of the duty cycle D on the basis of the error signal derived from this comparison. The operation of the compensator is periodical with a period referred to as *control cycle*. In integrated controllers the two cycles are coincident, that is the new value of D is computed by the compensator during the switching cycle and applied to the following one. However, depending on the implementation of the control cycle the control frequency may be lower than the switching frequency, that is

$$f_{control} = f_{sw} \tag{2}$$

Let us now first consider the main parameters of a switching power converter, which are basically the output regulation and the output noise. Then we will analyze the implementation choices which have been taken in the design of the experiment.

A. Output Regulation

The output regulation (OR) is the maximum variation of the D.C. output voltage from its nominal value and is the sum of two components, namely the line regulation considering the variations of the input load and the load regulation considering the variations of the load. The main factor affecting this parameter is the precision of the ADC (N_{ADC}), that the minimum variation of the output voltage which may be detected.

$$OR = V_{ADC} \cdot K \cdot 2^{-N_{ADC}} \tag{3}$$

The output regulation decreases by increasing the number N_{ADC} of bits of the ADC converter and for a precise output value a large value of N_{ADC} is required.

B. Output Noise

Although the output voltage is ideally constant there are A.C. noise components due both to parasitic parameters of components and to the digital operation of the controller which implies a quantization of the output to the DPWM and of the output of the ADC. The two main components are the Ripple noise (δV) and the Limit Cycle (LC) noise.

1) Ripple noise

The ripple noise is due to the A.C. component of the inductor current which flows in the output capacitor of the power stage and, due to the non-zero value of the Equivalent Series Resistance (shown as rC in fig. 1) of the capacitor, generates a variable voltage at the switching frequency f_sw. It is known in the literature that the peak value is equal to:

$$\triangle V = \triangle I \cdot ESR = \frac{V_{in} D(1-D)}{L \cdot f_{sw}} ESR \tag{4}$$

It may be easily verified that it has a maximum for $D = 0.5$ and the key point is that for a given value of inductance the noise decreases when the switching frequency is increased.

2) Limit Cycle noise The Limit Cycle (LC) noise derives from the fact that the output of the DPWM is quantized, that is the number of values of possible values of the duty cycle D is limited to $2^{N_{PWM}}$ where N_{PWM} is the number of bits controlling the modulator. The voltage difference between two output signals corresponding to duty cycles D_i and D_{i+1} is

$$\triangle V_i = V_{in} 2^{N_{PWM}} \tag{5}$$

If the target voltage is not equal to one of the quantized output levels the output voltage will oscillate between levels V_{oi} and V_{oi+1} because the controller tries to keep the output voltage equal to the target.

This oscillation takes place at a frequency equal to the control frequency or one subharmonic because the output averaging depends on many parameters such the filter cutoff

frequency, the controller setting, the load and also the amplitude of the ripple voltage. If the control frequency is far higher than the cutoff frequency of the filter, then the higher components of the LC noise will be filtered. A large research activity has been devoted to the reduction of the lower frequency components of this noise, mostly by dithering techniques [2,3,4] which aim to move these components to higher frequencies where they may be filtered. Unfortunately, these techniques may not be applied if the fundamental control frequency is of the same order of magnitude of the filter cutoff frequency.

The only other solution to cancel this noise is to avoid the oscillation between two different output levels. To obtain this the ADC quantization bin must be larger than the LSB of the Pulse Width Modulator (PWM) so at least one of the quantized DC output levels at a fixed duty cycle falls in the zero-error bin of the converter, i.e:

$$q_{ADC} = q_{PWM} \tag{6}$$

If the number of bits of the ADC is N_{ADC}, its reference voltage is V_R, the number of bits controlling the PWM modulator is N_{PWM} and the maximum input voltage V_{inMAX} the previous equation becomes:

$$\frac{V_{REF}}{2^{N_{ADC}}} > \frac{V_{inMAX}}{2^{N_{PWM}}} \tag{7}$$

If we assume that $V_R = V_{inMAX}$ then the condition for avoiding the limit cycle becomes:

$$N_{PWM} > N_{ADC} \tag{8}$$

This may be obtained by reducing the number of bits of the ADC, but it is clear from equation 3 that also the output regulation will be reduced.

C. Implementation choices

The design of a converter using a simple microcontroller must start from the consideration that a full realization in software is not feasible. The critical unit is the DPWM modulator whose straightforward implementation would be a nested loop of two counters, one for the duty cycle and one for the switching period. With $N_{PWM} = 8$ it would require a few thousands of instructions per switching cycle, leading to switching frequencies of the order of 4 kHz. According to equation (4) this would lead to a ripple noise of the order of 1V which is clearly unacceptable. Moreover, such a solution would use all the available CPU time voiding the possibility of performing other tasks in parallel.

For this reason, we took advantage of dedicated timer/counter unit of the ATmega328P processor which may directly implement a DPWM without software intervention. It is a counter which has two programmable thresholds. When the first one is reached an output pin is toggled from the high to the low level and when the second one is reached the counter is reset. The first threshold set the duty cycle and the second the switching frequency. The counter may be directly fed by the input clock at 16 MHz and the value of the second threshold it is possible to make a tradeoff between the number of bits N_{PWM} and the switching frequency f_{sw}. We chose for most of the experiments the combination with $N_{PWM} = 8$ and $f_{sw} = 64kHz$ with an expected ripple noise of 70mV in the worst case conditions.

The control loop has been implemented in software with a Proportional-Integrative (PI) compensator which performs a control cycle in approximately every 200 ms, out of which 100 ms are required to perform the analog to digital conversion. A maximum control frequency of 5 kHz may be expected and for any value under that we cannot expect the limit cycle noise to be filtered by the output filter at 1 kHz. We therefore chose to set the control frequency at 1 kHz using a timer interrupt. In such a way the control task takes 200 ms/1 ms = 20% of the total CPU time leaving 80% for other tasks.

IV MEASUREMENTS AND ANALYSIS

Two main set of measurements have been performed, the first one without limiting the effect of the limit cycle and the second one setting the condition indicated by equation 6.

In each measurement, the output voltage was set to a given value (ranging from 2 to 9) by setting the internal reference and then the input voltage varied, in steps of 1V from 10 to 18V.

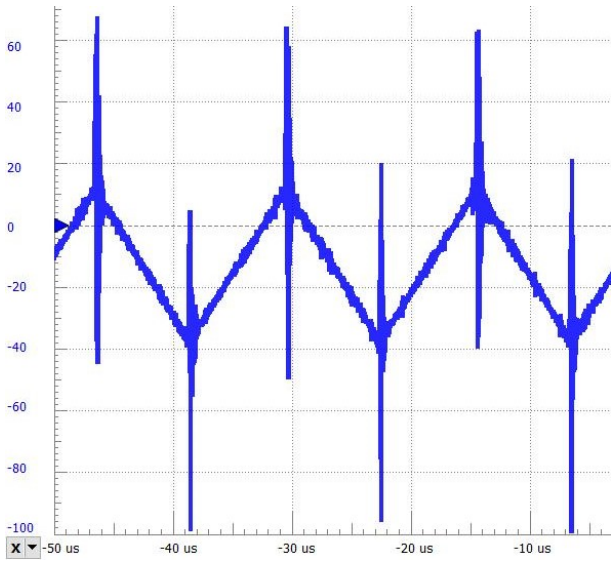

Fig. 2: Maximum ripple at switching

The first result is that the ripple voltage appears to be limited. Fig. 2 shows the ripple waveform for the maximum peak to peak case ($V_{in} = 18V, V_{out} = 9V$). In the picture, the voltage spikes are artifacts due to the coupling of the probe to the drivers of the gate switches. The value of the ripple is slightly lower than the predicted one, probably due to the lower value of the parasitic resistance of the capacitor.

The second result is that the LC noise is clearly present on the output as shown in the example of Fig.3 which was recorded in one of the measurements performed.

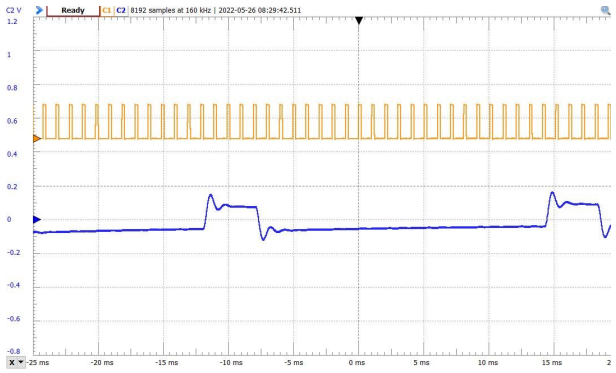

Fig. 3: Limit cycle noise

The top timing diagram of the figure is a signal synchronized to the control cycle. In this case the output is for 4 cycles at the upper value of the duty cycle and for 24 at the lower one. The table in fig. 4 shows the occurrence, and the peak value in mV of the LC noise, for all the combinations of the input and output voltages for which the measurements were taken.

V_{in} / V_{out}	10	11	12	13	14	15	16	17	18
2	0	0	0	0	0	0	0	0	120
3	0	0	0	0	80	0	0	0	130
4	0	0	0	70	0	0	0	0	150
5	0	60	0	70	0	0	0	0	150
6	0	0	0	0	0	0	0	100	0
7	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	90	100	0
9	0	0	0	0	70	0	90	0	0

Fig. 4: LC noise (in mV) for all V_{in} and V_{out} combinations

As clearly visible the noise is not present in all cases but only when the input and output values make a variation of one value of D change the output value of the ADC. It should be pointed out that since the noise is dependent on many parameters another measurement run could produce a very different picture.

Figure 5 shows the variation of the output voltage as a function of V_{in} for different output nominal values and the table of fig. 6 contains the maximum error e in mV with respect to the nominal value.

The output error and the line regulation appear to be satisfactory for most applications.

Another set of measurements was performed with a controller modified in order to cancel the LC noise according to equation 8. This has been obtained by masking the lower bits of the data acquired from the ADC, reducing in practice its precision. Fig. 7 shows the variation of the output voltage as a function of V_{in} and in the case of Fig. 8 the error with respect to the nominal value. As expected, the error is significantly larger, from 4 to 5 times, than in the previous case.

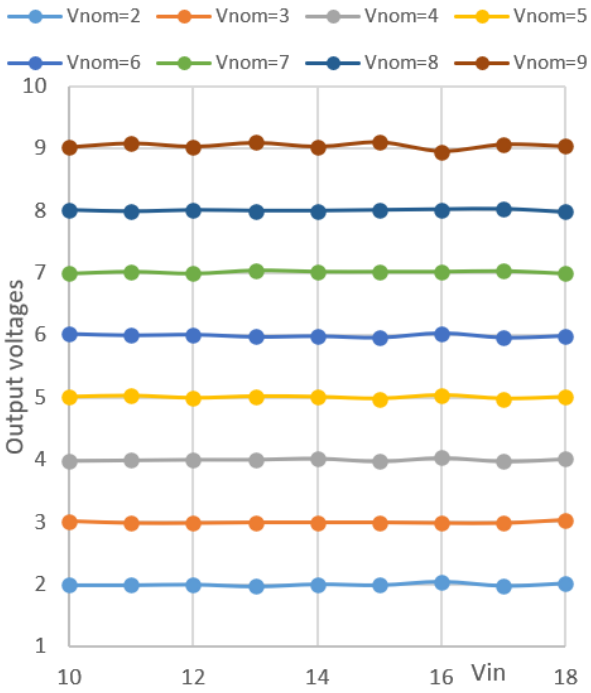

Fig. 5: V_{out} as a function of V_{in} for a non LC free setting

Vout	2	3	4	5	6	7	8	9
e	45	30	30	40	30	40	25	90

Fig. 6: Output error (mV) for a non LC free setting

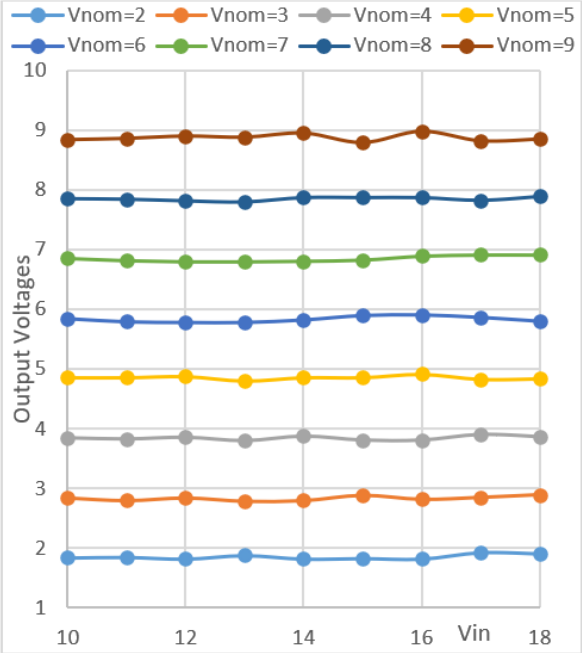

Fig. 7: V_u as a function of V_{in} for a LC free setting

Vout	2	3	4	5	6	7	8	9
e	180	200	200	200	210	200	200	200

Fig. 8: Output error e in mV for a LC free setting

V CONCLUSIONS AND DEVELOPMENTS

The paper has shown the design of the controller for a buck converter implemented using a popular and limited performance microcontroller and has the demonstrated that, taking advantage of the hardware characteristic of the processor it is possible to efficiently implement a power converter. The performance limits of the processor make it impossible to fully optimize the output characteristics of the converter.

In a real application, depending on the characteristics of the system to be implemented it is necessary to make a choice between a higher precision of the output D.C. value associated to a higher noise due to the limit cycle phenomenon and a lower output precision associated to a lower level noise.

The work described here requires to be extended to consider also the dynamic parameters of the converter such as the response to input voltage and load transients which have not fully investigated due to the requirements for more sophisticated measurement equipment.

VI REFERENCES

[1] L. Louis, "Working principle of Arduino and using it as a tool for study and research," International Journal of Control, Automation, Communication and Systems, vol. 1, no. 2, pp. 21-29, 2016.

[2] H. Peng, A. Prodic, E. Alarcon, and D. Maksimovic, "Modeling of quantization effects in digitally controlled DC–DC converters," IEEE Trans. Power Electron., vol.22, no. 1, pp. 208–215, Jan. 2007.

[3] J. Fang, X. Yang, L. Zhang, and Y. Tang, "An optimal digital pulse width modulated dither technique to enhance the resolution of high frequency power converters," IEEE Trans. Power Electron., vol. 32, no. 9, pp. 7222–7232, Sep. 2017.

[4] M. Usmonov, P. S. Crovetti, F. Gregoretti, and F. Musolino, "Suppression of quantization-induced limit cycles in digitally controlled DC-DC converters by dyadic digital pulse width modulation," in Proc. IEEE Energy Convers. Congr. Expo., Baltimore, MD, USA, 2019, pp. 2224–2231.